## ABSTRACT

A system and method to correct or cancel MOS linear region impedance curvature employing an analog solution to trim out the MOS linear region impedance curvature while accommodating PVT spreads in values of internal or external precision resistors. The linear region curvature correction may be obtained by using two MOS transistors in the pad driver/buffer and operating the transistors so as to proportionately increase output impedance of one of them when the output impedance of the other decreases, and vice versa. A linear pad impedance may be maintained over a range of Vpad values, while also maintaining the Vgs supplied to pad driver transistors at its maximum possible value to obtain greater linearity. The approach of the present disclosure relaxes the requirements on the voltage/current references used in the MOS pad drivers and makes tight impedance control possible, especially in a situation where the MOS fabrication process (typically all currently used processes) does not have available an internal precision resistor with a reasonably well controlled value.